REMARKS/ARGUMENTS

Claims 1-25 are pending in the present application. Claims 2, 3, 6, 8, 10, 11, 14, 16, 18, 19, 22, 24 and 25 have been amended herewith. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation

The Examiner rejected Claims 1-25 under 35 U.S.C. § 102(e) as being anticipated by Buch, U.S. Patent No. 6,901,522. This rejection is respectfully traversed.

For a prior art reference to anticipate in terms of 35 U.S.C. 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Applicants will now show that every element of the claimed invention is not identically shown in a single reference, and thus Claims 1-25 have been erroneously rejected under 35 U.S.C. § 102(e) as being anticipated by Buch.

Generally speaking with respect to Claim 1, such claim is directed to a time-based alteration of operation of a selected processor to reduce power usage. In particular, such claim recites "altering operation of the selected processor to reduce power usage *during the period of time*". The cited reference does not teach any usage of time or time dependence for achieving low power. Rather, a processor is instructed to run an OS idle loop in order to enter a low-power state (col. 4, lines 6-18), and then this processor is subsequently resumed to normal operation through another, separate call from a Java Virtual Machine to the operating system (col. 4, lines 19-31). This placing of a processor into, and then removing the processor from, a low power mode is *not time dependent or time based*, but instead is solely based on requisite processor computational power that is determined to be needed (col. 3, lines 34-65). Buch contemplates a processor load-based start and subsequent load-based stop of low power mode *without regards to time or time duration* (col. 3, lines 34-67). Thus, as every element of the claimed invention is not identically shown in a single reference – and in particular the claimed step of "altering operation of the selected processor to reduce power usage *during the period of time*" (where the call that is received from an operating system indicates that a selected processor in the set of processors is unneeded for such period of time) - it is urged that Claim 1 has been erroneously rejected under 35 U.S.C. § 102(e) as being anticipated by Buch.

Applicants initially traverse the rejection of Claims 2-8 for reasons given above with respect to Claim 1 (of which Claims 2-8 depend upon).

Further with respect to Claim 2, such claim recites that the call is a sub-processor partitioning call, which advantageously allows for use in a partitioned data processing system. In rejecting Claim 2, the Examiner cites Buch's teaching at col. 3, line 60 – col. 4, line 18 as teaching this claimed feature. It is urged that this passage merely describes that a 'system call' is made to the operating system (O/S) to set a

processor affinity level. There is no teaching of a sub-processor partitioning call, as expressly recited in Claim 2. In addition, Applicants urge that while Buch may describe a system having multiple processors, there is no teaching/suggestion of a multi-partitioned data processing system or a sub-processor partitioning call. Claim 2 has been amended to further emphasize this distinction, and thus it is urged that Claim 2 is not anticipated by the cited reference.

Further with respect to Claim 3, and for similar reasons to those given above with respect to Claim 1, the teachings of Buch do not contemplate a time-based duration for idle cycles, but instead contemplate a processor load-based start and subsequent load-based stop of low power mode – each as initiated by a unique system call based on current CPU load requirements (see, e.g. Buch col. 4, lines 19-31). Claim 3 has been amended to further emphasize this distinction, and thus it is urged that Claim 3 is not anticipated by the cited reference.

Further with respect to Claim 4 (and dependent Claim 5), and for similar reasons to those given above with respect to Claim 1, the teachings of Buch do not contemplate a time-based duration for returning a selected processor to the original state[1], but instead contemplate a processor load-based start and subsequent load-based stop of low power mode – each as initiated by a unique system call based on current CPU load requirements (see, e.g. Buch col. 4, lines 19-31). Thus, it is urged that Claim 4 (and dependent Claim 5) is not anticipated by the cited reference as every element of the claimed invention is not identically shown in a single reference.

Still further with respect to Claim 5, such claim recites "returning the selected processor to the original state if the period of time has not elapsed and an external interrupt indicating work is present for the selected processor is received". As can be seen, the selected processor is returned to the original state if two conditions are met – (1) the period of time has not elapsed and (2) an external interrupt indicating work is present for the selected processor is received. The cited reference does not teach or otherwise suggest such a two-fold conditional return to an original state. In rejecting Claim 5, the Examiner cites Buch's teaching at col. 4, lines 6-18 as teaching this claimed feature, which is alleged to be inherent in the ACPI Specification. Applicants urge that this cited passage and the ACPI discussion are with respect to processors *entering* a low power mode, and provide no teaching suggestion of exiting/resuming to a normal/original mode as per the features of Claim 5. Still further, there is no mention of any time-based resumption to a normal/original, as described above with respect to Claims 1 and 4. Thus, it is urged that Claim 5 is not anticipated by the cited reference as every element of the claimed invention is not identically shown in a single reference.

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[1] Claim 4 expressly recites "returning the selected processor to the original state *after the period of time has elapsed*" (emphasis added by Applicants).

Further with respect to Claim 6, such claim has been amended to emphasize the *multiple* operating system environments for which power management occurs. While the cited reference teaches multiple processors, it only contemplates a *single* operating system environment (Buch col. 3, lines 11-15; Figure 2, block 220). Thus, it is urged that Claim 6 is not anticipated by the cited reference as every element of the claimed invention is not identically shown in a single reference.

Further with respect to Claim 7, it is urged that the cited reference does not teach the claimed feature of "reducing a clock speed of the selected processor". In rejecting such claim, the Examiner states that such feature is inherent in the ACPI Specification. Applicants urge that such claimed feature is *not* inherent in the teachings of the cited reference. "Inherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) (quoting *Hansgirg v. Kemmer*, 102 F.2d 212, 214, 40 USPQ 665, 667 (CCPA 1939)). "To establish inherency," the Federal Circuit recently stated, "the extrinsic evidence `must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.'" *In re Robertson*, 169 F.3d 743, 745 [49 USPQ2d 1949] (Fed. Cir. 1999); see also *Continental Can Co. U.S.A., Inc. v. Monsanto Co.*, 948 F.2d 1264, 1268 [20 USPQ2d 1746] (Fed. Cir. 1991). Such inherency may not be established by "`probabilities or possibilities.'" *Continental Can*, 948 F.2d at 1269 (quoting *In re Oelrich*, 666 F.2d 578, 581 [212 USPQ 323] (C.C.P.A. 1981)). Because the cited reference describes that low power mode is achieved by placing the processor in a mode that is running an OS idle loop (col. 4, lines 6-10), reducing clock speed to achieve low power is not inherent in the teachings of the cited reference as power reduction is achieved using a different procedure and therefore the extrinsic evidence does *not* make it clear that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill.

Further, in relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); *In re Oelrich*, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); *In re Wilding*, 535 F.2d 631, 190 USPQ 59 (CCPA 1976); *Hansgirg v. Kemmer*, 102 F.2d 212, 40 USPQ 665 (CCPA 1939). The Examiner provides no basis in fact to support the inherency allegation – instead merely stating "Reducing a clock speed of the selected processor is inherent in the ACPI Specification", which fails to meet the burden of proof requirements of the Federal Circuit to properly establish inherency.

Thus, Applicants have shown numerous errors in the Examiner's inherency assertion with respect to Claim 7, and therefore urge that such claim has been erroneously rejected.

Further with respect to Claim 8, such claim has been amended to specify use of a threshold to conditionally place a processor in a sleep mode, which advantageously allows for taking into account various overhead delays that may be encountered when placing a processor in a power saving mode (Specification page 18, last paragraph). The cited reference does not teach or otherwise contemplate such a threshold. Still further, Buch's low power mode is not time-based, as previously described above with respect to Claims 1 and 4. Thus, it is further urged that Claim 8 is not anticipated by the cited reference as every element of the claimed invention is not identically shown in a single reference.

Applicants traverse the rejection of Claims 9-25 for similar reasons to those given above with respect to Claims 1-8.

Therefore, the rejection of Claims 1-25 under 35 U.S.C. § 102(e) has been overcome.

II. Conclusion

It is respectfully urged that the subject application is patentable over the cited reference and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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